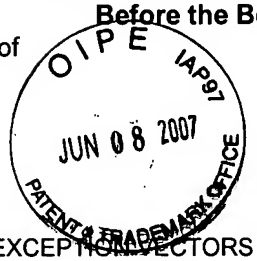
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences



In re Patent Application of
BURDASS, A.
Serial No. 10/798,890
Filed: March 12, 2004
Title: PREFETCHING EXCEPTION VECTORS

Atty Dkt. SCS-550-530
C# M#
TC/A.U.: 2183
Examiner: B. Johnson
Date: June 8, 2007

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

☐ **Correspondence Address Indication Form Attached.**

☐ **NOTICE OF APPEAL**
Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the Examiner twice/finally rejecting applicant's claim(s). $500.00 (1401)/$250.00 (2401) $

☒ An appeal **BRIEF** is attached in the pending appeal of the above-identified application $500.00 (1402)/$250.00 (2402) $ 500.00

☐ Credit for fees paid in prior appeal without decision on merits -$ ( )

☐ A reply brief is attached. **(no fee)**

☐ Petition is hereby made to extend the current due date so as to cover the filing date of this paper and attachment(s)
One Month Extension $120.00 (1251)/$60.00 (2251)
Two Month Extensions $450.00 (1252)/$225.00 (2252)
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TOTAL FEE ENCLOSED $ 500.00

Any future submission requiring an extension of time is hereby stated to include a petition for such time extension. The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our **Account No. 14-1140.** A duplicate copy of this sheet is attached.

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Signature:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of	Confirmation No.: 4902
BURDASS	Atty. Ref.: 550-530
Serial No. 10/798,890	Group: 2183
Filed: March 12, 2004	Examiner: B. Johnson
For: PREFETCHING EXCEPTION VECTORS	

* *

APPEAL BRIEF

On Appeal From Group Art Unit 2183

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of

BURDASS, A. Atty. Ref.: 550-530

Serial No. 10/798,890 Group: 2183

Filed: March 12, 2004 Examiner: B. Johnson

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* *

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APPEAL BRIEF

Sir:

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified appeal is ARM Limited by virtue of an assignment of rights from the inventor to ARM Limited recorded July 13, 2004 at Reel 15564, Frame 134.

II. RELATED APPEALS AND INTERFERENCES

There are believed to be no related appeals, interferences or judicial proceedings with respect to the present application, other than the Pre-Appeal Brief Request for Review filed February 27, 2007.

III. STATUS OF CLAIMS

Claims 1-8 and 16-23 have been cancelled without prejudice. Claims 9-15 and 24-30 stand rejected in the outstanding Final Official Action. The Examiner contends that claims 9-12 and 24-27 are anticipated under 35 USC §102 by Birk (U.S. Patent 6,978,350). With respect to claims 13 and 28, the Examiner contends that these are obvious under 35 USC §103 over Birk in view of Nguyen (U.S. Patent 5,481,685). With respect to claims 14, 15, 29 and 30, the Examiner contends that these claims are obvious under 35 USC §103 over Birk in view of Glass (U.S. Patent 5,784,602). The above rejections of claims 9-15 and 24-30 are appealed.

IV. STATUS OF AMENDMENTS

No further response has been submitted with respect to the Final Official Action in this application other than the filing of a Pre-Appeal Brief Request for Review which decision was mailed May 8, 2007 (Paper No. 20070503).

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Appellant's specification and figures provide an explanation of the claimed invention set out in independent claims 9 and 24, with each claimed structure and method step addressed as to its location in the specification and in the figures.

"9. Apparatus for processing data [system 2 shown in figure 1 and discussed on page 7, lines 9-22 and elsewhere in the specification], said apparatus comprising:

a cache memory [block 6 shown in figure 1 and discussed on page 7, lines 9-22 and elsewhere in the specification] operable to store program instructions to be executed;

an instruction pipeline [system 20 shown in figure 1 and discussed on page 7, lines13-22 and elsewhere in the specification] including an instruction prefetch unit [block 24 shown in figure 1 and discussed on page 7, lines 24 to page 8, line 3 and elsewhere in the specification]; and

an exception controller [block 26 shown in figure 1 and discussed on page 7, line 27 to page 8, line 3 and elsewhere in the specification], responsive to an exception signal signaling an exception, for triggering exception processing by forcing program execution starting from an exception handling program instruction [discussed on page 7, line 31 to page 8, line 11 and elsewhere in the specification] stored at a predetermined memory location; wherein upon receipt of said exception signal part way through execution of a current program instruction, said exception controller triggering a lookup of said exception handling program instruction within said cache memory [discussed on page 7, line 34 to page 8, line 11 and elsewhere in the specification] and, if said exception handling program instruction is not present within said cache memory, triggering a cache linefill

operation [discussed on page 7, line 34 to page 8, line 11 and elsewhere in the specification] to read said exception handing program instruction from a main memory [block 8 as shown in figure 1 and discussed on page 7, lines 9-22 and elsewhere in the specification] to said cache memory [6], and, upon completion of execution of said current program instruction, if said exception is still current, then said instruction prefetch unit fetches said exception handling program instruction from said cache memory [discussed on page 8, lines 13-16 and elsewhere in the specification]."

"24. A method of processing data, said method comprising the steps of:

storing program instructions to be executed within a cache memory [block 6 shown in figure 1 and discussed on page 7, lines 9-22 and elsewhere in the specification];

processing program instructions with an instruction pipeline [system 20 shown in figure 1 and discussed on page 7, lines13-22 and elsewhere in the specification] including an instruction prefetch unit [block 24 shown in figure 1 and discussed on page 7, lines 24 to page 8, line 3 and elsewhere in the specification]; and

triggering, in response to an exception signal [step 28 shown in figure 3 and discussed on page 9, lines 12-26 and elsewhere in the specification], exception processing by forcing program execution starting from an exception handling

program instruction stored at a predetermined memory location; wherein, upon receipt of said exception signal part way through execution of a current program instruction, said triggering step includes triggering a lookup [step 30 shown in figure 3 and discussed on page 9, lines 12-26 and elsewhere in the specification] of said exception handling program instruction within said cache memory [6 as shown in figure 1 and discussed on page 7, line 34 to page 8, line 11 and elsewhere in the specification] and, if said exception handling program instruction is not present within said cache memory [6], said triggering step includes triggering a cache linefill operation [discussed on page 7, line 34 to page 8, line 11 and elsewhere in the specification] to read said exception handing program instruction from a main memory [8] to said cache memory [6], and, upon completion of execution of said current program instruction, if said exception is still current, then said instruction prefetch unit fetches said exception handling program instruction from said cache memory[discussed on page 8, lines 13-16 and elsewhere in the specification]."

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 9-12 and 24-27 stand rejected under 35 USC §102 as being anticipated by Birk (U.S. Patent 6,978,350).

Claims 13 and 28 stand rejected under 35 USC §103 as unpatentable over Birk in view of Nguyen (U.S. Patent 5,481,685).

Claims 14, 15, 29 and 30 stand rejected under 35 USC §103 as unpatentable over Birk in view of Glass (U.S. Patent 5,784,602).

VII. ARGUMENT

Appellant's arguments include the fact that the burden is on the Examiner to first and foremost properly construe the language of the claims to determine what structure and/or method steps are covered by that claim. After proper construction of the claim language, the burden is also on the Examiner to demonstrate where a single reference (in the case of anticipation) or a plurality of references (in the case of an obviousness rejection) teaches each of the structures and/or method steps recited in independent claims 9 and 24.

The Court of Appeals for the Federal Circuit has noted in the case of *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984) that "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."

Furthermore, the Court of Appeals for the Federal Circuit has stated in the case of *In re Rouffet*, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998)

> to prevent the use of hindsight based on the invention to defeat patentability of the invention, this court **requires** the examiner to show a **motivation** to combine the references that create the case of obviousness. In other words, the Examiner **must show reasons** that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. (Emphasis added).

A. The Examiner fails to identify where the Birk reference teaches "upon completion of execution of said current program instruction . . ." said instruction prefetch unit fetches said exception handling program instructions

Appellant's independent claims 9 and 24 both specify the conditional phrase that, upon "completion of execution of said current program instruction" certain other specified actions take place ("upon completion of execution of sid current program instruction, if said exception is still current, then said instruction prefetch unit fetches said exception handling program instruction from said cache memory." See Claims 9 and 24)

The Examiner alleges that this conditional phrase is disclosed in Birk at Col. 2, lines 36-49. However, a review of these lines indicates that there is no such conditional phrase disclosed in the Birk reference. In fact the cited portion of Birk says nothing about any aspect of "upon completion of execution of said current program" The Examiner fails to disclose where this claimed conditional interrelationship between claimed elements is taught in Birk.

In fact, he apparently fails to appreciate the Birk actually teaches the direct opposite of this claim requirement. Birk at column 3, lines 59-63, states that "since the DSP 10 aborts the instructions in the pipeline upon detection of an interrupt, **it aborts the instruction** which generated the cache line miss and begins execution of the interrupt service routine." (emphasis added). Accordingly, the instruction in Birk is not completed (contrary to the claimed requirement of "upon completion"), and this failure to complete is necessary for the proper operation of the Birk reference. Birk does not explain how it is able to tolerate aborting such a partially completed instruction.

As explained in detail on page 4, lines 1-12 of the present specification, the claimed invention initiates the cache line fill operation to read the exception handling program instruction from main memory partway through execution of the current program instruction, but does not fetch that instruction from the cache memory until completion of the current program instruction. Thus, Birk, which teaches instruction abortion, clearly does not have Appellant's claimed exception controller which is dependent upon "**completion** of execution of said current program instruction." (Emphasis added).

Thus, the Examiner has not indicated how or where the Birk reference teaches Appellant's conditional controller, i.e., "upon completion of execution of said current program instruction." Clearly, the Birk reference requires the direct opposite of

Applicant's claimed exception controller which requires abortion of "the instructions in the pipeline upon detection of an interrupt." (Column 3, lines 60-61).

It should also be noted that nowhere in the Final Rejection does the Examiner allege any other prior art reference of record to disclose the conditional phrase which is clearly missing from Birk. Thus no reference of record discloses this claimed feature.

The burden is on the Examiner to clearly demonstrate where this claimed (in independent claims 9 and 24) interrelationship is disclosed in Birk and has failed to meet this burden.

B. The Examiner's assertion on page 3, first full paragraph is completely unsupported by the Birk reference

It would appear that the Examiner misunderstands the manner of operation as disclosed in the Birk reference. For example, the Examiner states on page 3, lines 4-5 of the Final Rejection that "[n]ote that the instruction service routine comprises a plurality of instructions. So, it follows the memory hierarchy outlined in col 2 lines 36-49."

This contention by the Examiner is traversed and, in fact, is contrary to what one of ordinary skill in the art would understand when reading the Birk reference. The whole point of the Birk disclosure is to avoid the stall cycles associated with a miss in the cache memory. Instead, Birk suggests that, when

executing a normal program instruction from a given program thread, if a miss occurs, then this should trigger processing to be started from another program thread so that the stall associated with the cache miss can be avoided.

In order to achieve this desired behavior, which is the whole reason for the arrangement of Birk, it is necessary that the instruction of the ISR or the different thread should be present within the cache memory and not itself result in a second cache miss. There is no point in using the system of Birk if one cache miss is avoided merely to result in another cache miss.

It will be appreciated by those of ordinary skill in the art that Birk could readily arrange for the ISR or other thread code to be guaranteed present within the memory by, for example, using a cache lockdown technique for such code. The assertion by the Examiner that the interrupt service routine will follow the normal memory hierarchy within Birk and accordingly will require fetching to the cache memory is completely unsupported speculation on the Examiner's part and, in fact, contrary to the purpose of Birk.

Thus, the Examiner's conclusion that Birk teaches a plurality of instructions which will follow the memory hierarchy outlined in column 2, lines 36-49 is simply wrong and actually contrary to the disclosure contained in Birk. Again, if Birk contained any such disclosure, the Examiner would be able to point to that disclosure as an example. The Examiner has failed to so indicate and

therefore fails to meet his burden of proving that the contended structure, method step and/or interrelationship is actually in the Birk reference.

C. The Examiner misapprehends claims 9 and 24 and, as a result, appears to ignore the "if . . . , then . . ." conditionality expressed therein

The Examiner construes the "if . . . , then . . ." element interrelationship of claims 9 and 24 to be met if, as he argues in the Final Rejection, page 3, lines 12-14, the Birk teaching discloses that the behavior takes place **both** if the exception is still current and if the exception is not still current. This is believed to be an improper interpretation of this portion of Appellant's claim.

The claim language positively recites "upon completion of execution of said current program instruction, **if said exception is still current, then said instruction prefetch unit fetches** . . . ." The Examiner has provided no support for his misinterpretation of the claim language which clearly states that "if said exception is still current, then said instruction prefetch unit fetches."

Not only has the Examiner misinterpreted the claim language, but he has failed to identify where there is any equivalent teaching in Birk. There is certainly no identification that an exception controller having the claimed interrelationship is disclosed in the Birk reference.

It should also be noted that nowhere in the Final Rejection does the Examiner allege any other prior art reference of record to disclose the "if . . . , then . . ."

interrelationship which is clearly missing from Birk. Thus no reference of record discloses this claimed feature.

Birk fails to disclose all claimed features of the independent claims 1 & 24, as well as those dependent thereon.

D. The Examiner provides no "reason" or "motivation" for combining the Birk and secondary references

As is well known, examiners are not free to merely pick and choose elements from different references and combine them in the manner taught only by Appellant's claims. Rather, the Court of Appeals for the Federal Circuit, as noted above in the *In re Rouffet* decision, has consistently held that the burden is on the examiner to establish some "reason" or "motivation" for combining elements of two prior art references.

The requirement that the Examiner identify some "reason" for combining elements has also been reaffirmed by Deputy Commissioner Focarino in her May 3, 2007 memo stating that "in formulating a rejection under 35 USC §103(a) based upon a combination of prior art elements, it remains necessary [for an examiner] to identify the reason why a person of ordinary skill in the art would have combined the prior art elements in the manner claimed."

The requirement for some "reason" or "motivation" for combining elements was pointed out to the Examiner (Amendment filed September 14, 2006 on page

10), the Examiner's statement that one skilled in the art would have been motivated to make the combination based on the reasoning disclosed in Glass (i.e., that an integrated circuit is "highly advantageous for space, speed, power consumption and cost reasons" (Glass, column 4, lines 23-25)) does not provide any reason or motivation. Using an integrated circuit does provide some of the stated advantages, but the Examiner has not indicated how or where there is any reason or motivation to pick and chose the elements from the Birk/Glass or Birk/Nguyen combinations of references and combine them in the manner of Applicant's claims. While some advantages of integrated circuits are identified, the required reason and motivation for combining elements is still missing.

In sum, the Examiner has articulated no "reason" why one would adopt the claimed elements or their claimed interrelationships as set out in independent claims 9 and 24.

E. The Examiner ignores the fact that Birk teaches away from Appellant's claimed combination

As noted above, Birk teaches the abortion of the instruction which generated the cache line miss and thus the instruction **is not completed**. As noted, this is the direct opposite of Appellant's claimed requirement "upon **completion of execution** of said current program instruction." (emphasis added). Thus, Birk,

in teaching the direct opposite of Appellant's claimed exception controller, would tend to lead one of ordinary skill in the art away from Appellant's invention.

The Federal Circuit has also opined that it is "error to find obviousness where references 'diverge from and teach away from the invention at hand'." *In re Fine*, 5 USPQ2d 1596, 1599 (Fed. Cir. 1988). As noted above, Birk specifically teaches away from the claimed invention.

Moreover, the Examiner has failed to explain how or why one of ordinary skill in the art would ignore this contrary teaching of Birk when attempting to make the combination of Birk with either Nguyen or Glass in the rejections of claims 13-15 and 28-30. As a consequence, neither of these combinations would be obvious in view of the Birk reference.

F. The Examiner fails to set out a *prima facie* case of anticipation of claims 9-12 and 24-27 by Birk under the provisions of 35 USC §102

In the remaining sections F-H, in order to avoid duplication of previous sections, Appellant will refer to and incorporate by reference, any previously noted and pertinent section.

As noted above, it is incumbent upon the Examiner to establish where "each and every element of the claimed invention, arranged as in the claim" is disclosed in the Birk reference in order to set out a prima facie case of anticipation under 35 USC §102. As noted above in section A, the Examiner doesn't establish

where the claimed condition phrase "upon completion of execution" is disclosed in the Birk reference. Additionally, in section C the Examiner has failed to indicate where the claimed "if . . . , then . . ." interrelationship is disclosed in Birk. Moreover, in section B it is established that the Examiner misunderstands the disclosure of the Birks reference and in section E it is demonstrated that Birk actually teaches away from at least one of the claimed limitations alleged to be disclosed by Birk.

Because there is no rational basis for concluding that "each and every element of the claimed invention, arranged as in the claim" is disclosed in Birk, the rejection of independent claims 9 and 24 and claims 10-15 and 25-30 dependent thereon, respectively, of necessity fails.

G. The Examiner fails to set out a *prima facie* case of obviousness of claims 13 and 28 in view of Birk and Nguyen under the provisions of 35 USC §103

1. The Examiner fails to meet his burden of showing where the prior art discloses claimed elements, method steps and/or interrelationships

In addition to *In re Rouffet* above, the Examiner is reminded that the Court of Appeals for the Federal Circuit has held that "the PTO has the burden under Section 103 to establish a *prima facie* case of obviousness." *In re Fine* at 1598. "It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *Id.*

As noted in sections A and C, at least two claimed structures or structural interrelationships are not disclosed in the Birk reference or in any other cited prior art reference. Because all claimed elements are not disclosed in an combination of prior art, the rejection under 35 USC §103 fails, even if one were to combine prior art references.

2. The Examiner fails to articulate any reason for combining references

Furthermore, as noted in section D above, the Examiner fails to provide any reason for combining elements from any references. Neither the primary Birk reference or the secondary Nguyen reference is even alleged to contain any "reason" for combining references.

As a result of the above, there is no basis for any *prima facie* case of obviousness of independent claims 9 and 24 or claims 10-15 and 25-30 dependent thereon.

3. The Examiner fails to explain why Birk would not lead those of ordinary skill away from the claimed invention

Finally, as noted in section E above, the Birk reference clearly would lead one of ordinary skill in the art away from the invention in independent claims 9 and 24. As a result, even if a *prima facie* case of obviousness was made out (and this is strenuously traversed), this evidence clearly rebuts any such case and instead evidences the non-obviousness of the claimed combination.

As a result of Birk leading those of ordinary skill away from the claimed invention, independent claims 9 and 24 and claims dependent thereon are non-obvious in view of Birk by itself or in combination with Nguyen.

H. The Examiner fails to set out a *prima facie* case of obviousness of claims 14, 15, 29 and 30 in view of Birk and Glass under the provisions of 35 USC §103

All of the above comments in sections A-G regarding the Birk reference are incorporated by reference. The Examiner has made no allegation that Glass supplies the disclosures noted to be missing from Birk. Thus he has failed to establish that all claimed elements, method steps and/or interrelationships are disclosed somewhere in the prior art. As a result, just as in section G, even if combined, the Birk and Glass references do not disclose all of the claim limitations and therefore the rejection over Birk/Glass fails.

Moreover, the Examiner has identified no "reason" for combining these references and thus no *prima facie* case of obviousness has been made out. Where is there any allegation that one of ordinary skill would be motivated to combine the Birk and Glass references? There is none that goes to any characteristic of either reference which would motivate the combination. Therefore, no *prima facie* case is made out in the Final Rejection.

In fact, as noted above in section E, Birk would lead one of ordinary skill away from any such claimed combination. Thus, the primary reference "teaching

away" from the claimed combination clearly rebuts any *prima facie* case of obviousness.

Accordingly there is no basis for rejecting independent claims 9 and 24, or any claims dependent thereon, under 35 USC §103 over the Birk and Glass combination of references.

VIII. CONCLUSION

As demonstrated above, at least two specifically enumerated claimed structures, method steps and/or interrelationships are clearly missing in the Birk and other prior art references. The Examiner fails to identify where the Birk reference teaches "upon completion of execution of said current program instruction . . ." (claim 1, line 12 and claim 24, line 14), or the conditional phrase "if said exception is still current, then . . ."(claim 1, line 13 and claim 24, lines 14-15). The Examiner apparently misunderstands what is and is not taught and disclosed in the Burk reference. Additionally, the Examiner has ignored the requirements to show both a reason for combining prior art (even if it did contain a disclosure of claimed elements, method steps and/or interrelationships) as well as some rationale for ignoring the contrary teachings of Birk.

As a result of the above, there is simply no support for the rejections of Appellant's independent claims or claims dependent thereon under 35 USC §102 or §103. Thus, and in view of the above, the rejection of claims 9-15 and 24-30

under 35 USC §§102 and 103 is clearly in error and reversal thereof by this Honorable Board is respectfully requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____

Stanley C. Spooner
Reg. No. 27,393

SCS:kmm
Enclosure

IX. CLAIMS APPENDIX

1 – 8 (cancelled).

9. (currently amended) Apparatus for processing data, said apparatus comprising:

a cache memory operable to store program instructions to be executed;

an instruction pipeline including an instruction prefetch unit; and

an exception controller, responsive to an exception signal signaling an exception, for triggering exception processing by forcing program execution starting from an exception handling program instruction stored at a predetermined memory location; wherein upon receipt of said exception signal part way through execution of a current program instruction, said exception controller triggering a lookup of said exception handling program instruction within said cache memory and, if said exception handling program instruction is not present within said cache memory, triggering a cache linefill operation to read said exception handing program instruction from a main memory to said cache memory, and, upon completion of execution of said current program instruction, if said exception is still current, then said instruction prefetch unit fetches said exception handling program instruction from said cache memory.

10. (original) Apparatus as claimed in claim 9, wherein execution of said current instruction lasts for a plurality of clock cycles and lookup of said exception handling program instruction within said cache memory starts part way through said plurality of clock cycles.

11. (original) Apparatus as claimed in claim 9, wherein said exception handling program instruction redirects program execution to an exception handling routine.

12. (original) Apparatus as claimed in claim 9, wherein said exception controller is an interrupt controller, said exception signal is an interrupt signal and said exception handling program instruction is and interrupt handling program instruction.

13. (original) Apparatus as claimed in claim 9, wherein said exception is one of a data abort and a prefetch abort.

14. (original) Apparatus as claimed in claim 9, wherein said cache memory and said exception controller are parts of a processor core.

15. (original) Apparatus as claimed in claim 9, wherein said apparatus is an integrated circuit.

16. (cancelled).

17. (cancelled).

18. (cancelled).

19. (cancelled).

20. (cancelled).

21. (cancelled).

22. (cancelled).

23. (cancelled).

24. (currently amended) A method of processing data, said method comprising the steps of:

storing program instructions to be executed within a cache memory;

processing program instructions with an instruction pipeline including an instruction prefetch unit; and

triggering, in response to an exception signal, exception processing by forcing program execution starting from an exception handling program instruction stored at a predetermined memory location; wherein, upon receipt of said exception signal part way through execution of a current program instruction,

said triggering step includes triggering a lookup of said exception handling program instruction within said cache memory and, if said exception handling program instruction is not present within said cache memory, said triggering step includes triggering a cache linefill operation to read said exception handing program instruction from a main memory to said cache memory, and, upon completion of execution of said current program instruction, if said exception is still current, then said instruction prefetch unit fetches said exception handling program instruction from said cache memory.

25. (original) A method as claimed in claim 24, wherein execution of said current instruction lasts for a plurality of clock cycles and lookup of said exception handling program instruction within said cache memory starts part way through said plurality of clock cycles.

26. (original) A method as claimed in claim 24, wherein said exception handling program instruction redirects program execution to an exception handling routine.

27. (original) A method as claimed in claim 24, wherein said exception signal is an interrupt signal and said exception handling program instruction is and interrupt handling program instruction.

28. (original) A method as claimed in claim 24, wherein said exception is one of a data abort and a prefetch abort.

29. (original) A method as claimed in claim 24, wherein said method is performed within a processor core.

30. (original) A method as claimed in claim 24, wherein method is performed within an integrated circuit.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.